
# Verification Challenges for Retimers

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# Disclaimer

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# Challenges With High Frequency

- **Channel Fading**
  - Higher frequency means greater channel loss.
  - Trace length getting reduced from 20’’ in PCIe® 3.0 to 12’’ in PCIe 4.0
- **Signal quality at Receiver end**
  - High frequency signal meaning higher jitter implications, higher signal loss and distortion
  - PCIe 4.0 demands an eye height of 15 mV after equalization and a maximum BER of  1X10-12
- **Signal Integrity**
  - Higher frequency signal indicate more signal integrity challenges like cross talk

# What is a Retimer?

- **Retimers**
  - Physical layer devices that fine tune the signal using CTLE (Continuous Time Linear Equalization) and transmit using FIR
  - Increase signal transmission length
  - Minimize jitter
  - Reduce cross talk and reflections

# What is a Retimer?

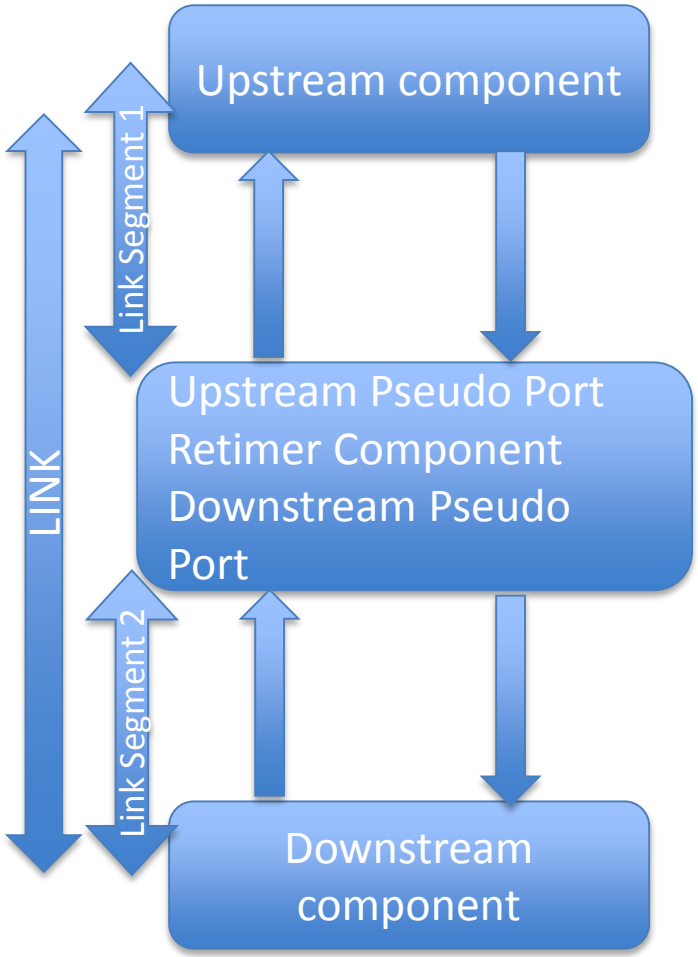
- **Requirements**
  - Comply with electrical specification
  - De-skew symbols
  - Determine port orientation
  - Perform lane polarity inversion
  - Execute link equalization procedure
  - Pass loopback data between loopback master and slave
  - Generate compliance pattern
  - Infer Electrical Idle at all data rates
  - Perform clock compensation via addition or removal of SKPs
  - Support L1

# Retimer

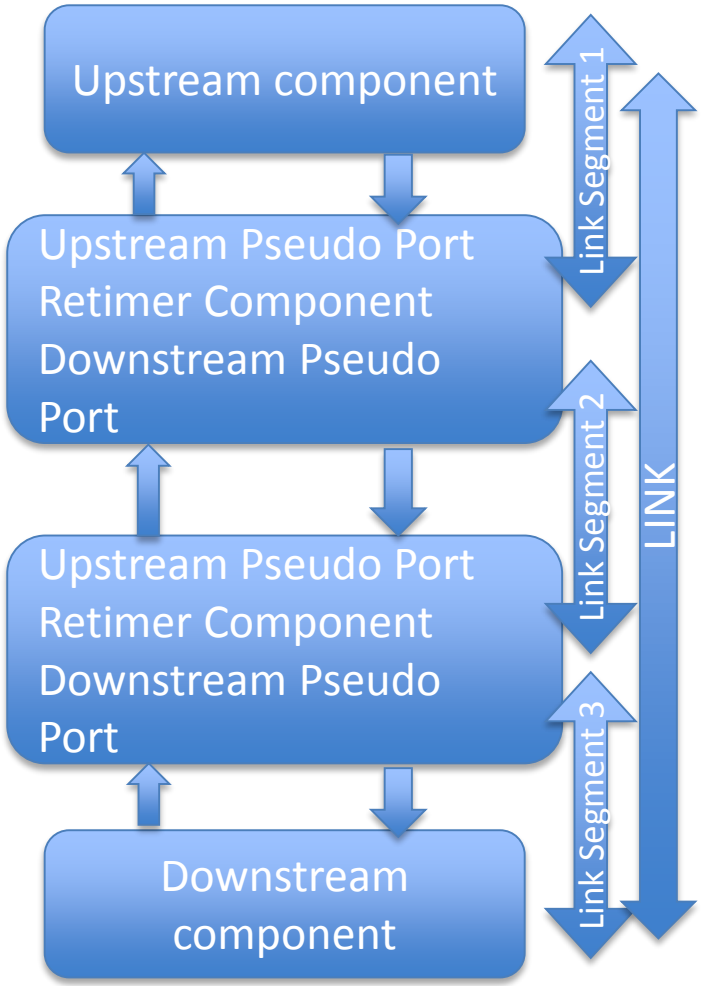
- **Supported Topology**
  - Forwarding mode
    - Symbols are forwarded on each upstream and downstream path
  - Execution mode
    - Upstream pseudo port act as upstream component
    - Downstream pseudo port act as downstream component

# Retimer: Topology

## Forwarding mode




## Execution mode



# Retimer

- **Rules**
  - Forwarding Mode Rules
    - Orientation and Lane number
    - Electrical Idle Entry
    - Electrical Idle Exit
    - Data Rate Change
    - Ordered set Modification
    - DLLP/TLP/Logical Modification
    - Encoding and Scrambling
    - Link Disable and Hot Reset Entry
    - Compliance Receive and Enter Compliance

# Retimer

- **Rules**
  - Ordered set Modification
    - Modify certain pre-specified ordered sets
    - Modify LS/FS values in both directions
    - Modify preC/postC/C values in both directions
    - Parity
    - Transmitter Presets and Receiver hints
    - SKP ordered sets
  - DLLP/TLP/Logical Modification
    - No modification to DL and TL packets

# Retimer

- **Rules**
  - Execution Mode Rules
    - CompLoadBoard
    - Link Equalization
      - Downstream Lanes
      - Upstream Lanes
    - Retimer Latency

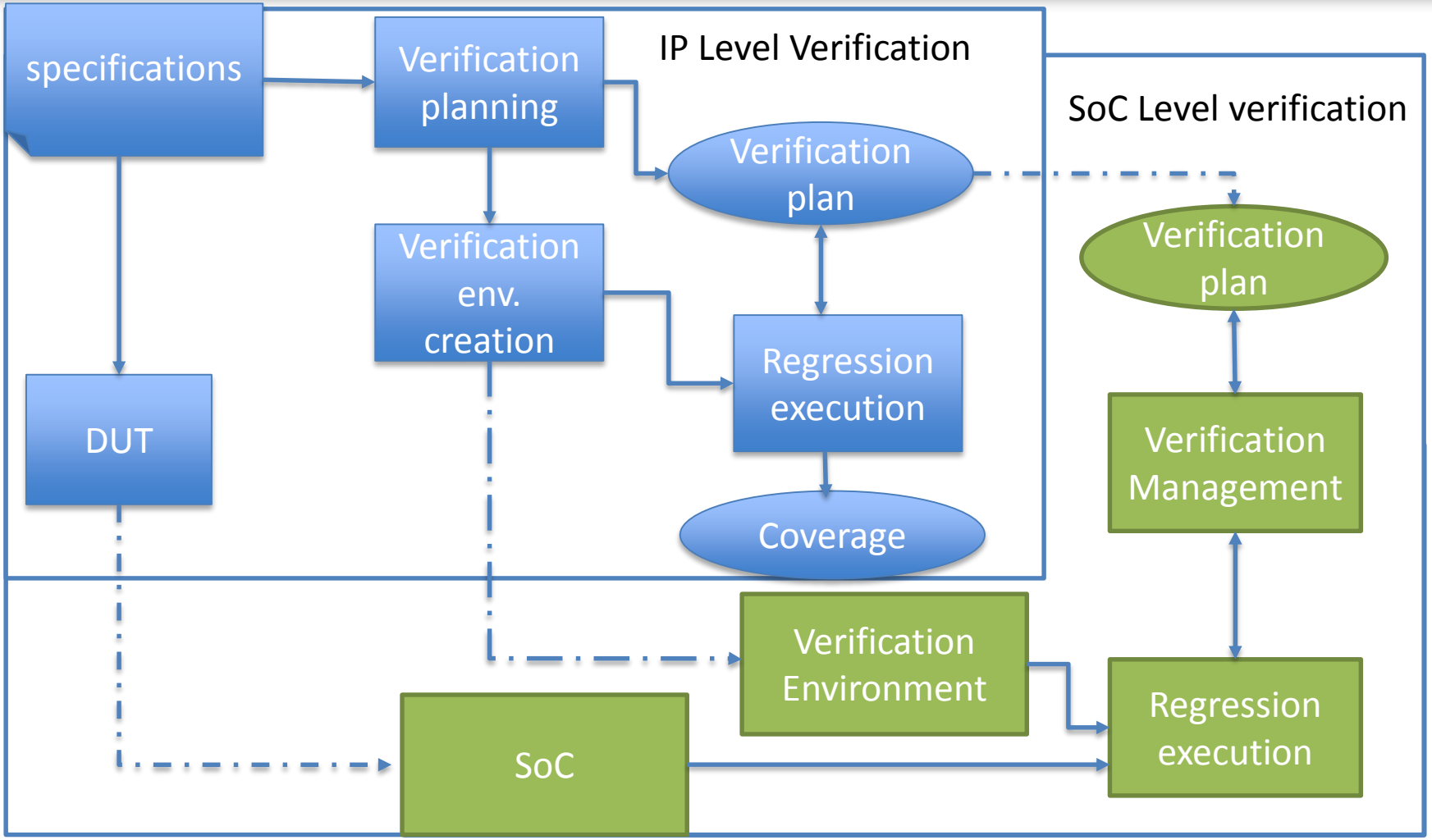
# Verification Challenges

- Have I done enough verification?
- Time to market and total cost
- Silicon Respin

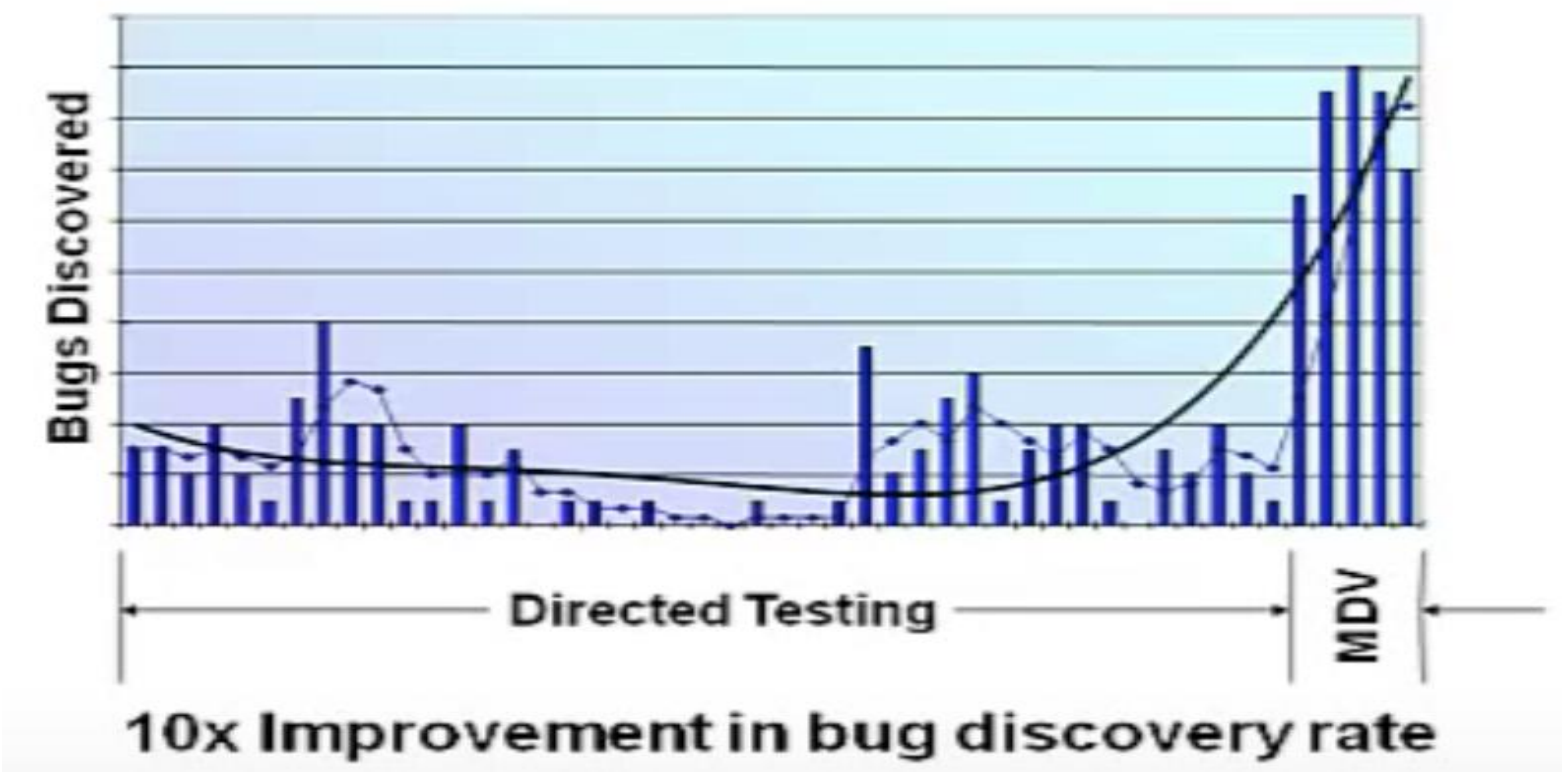
# Verification Challenges: Solution

- **Traditional Approach**
  - Higher control for targeting specific feature
  - Writing and debugging hundreds and thousands of tests
  - No measure to find if the verification is comprehensive
  - High maintenance cost
- **Metric Driven Verification**
  - Measure design coverage and hence provides predictability
  - Better focus, greater visibility into the issues
  - Quality improvement
  - Reuse at SoC level

# Environment Reuse



# 10x Improvement in Bug Discovery



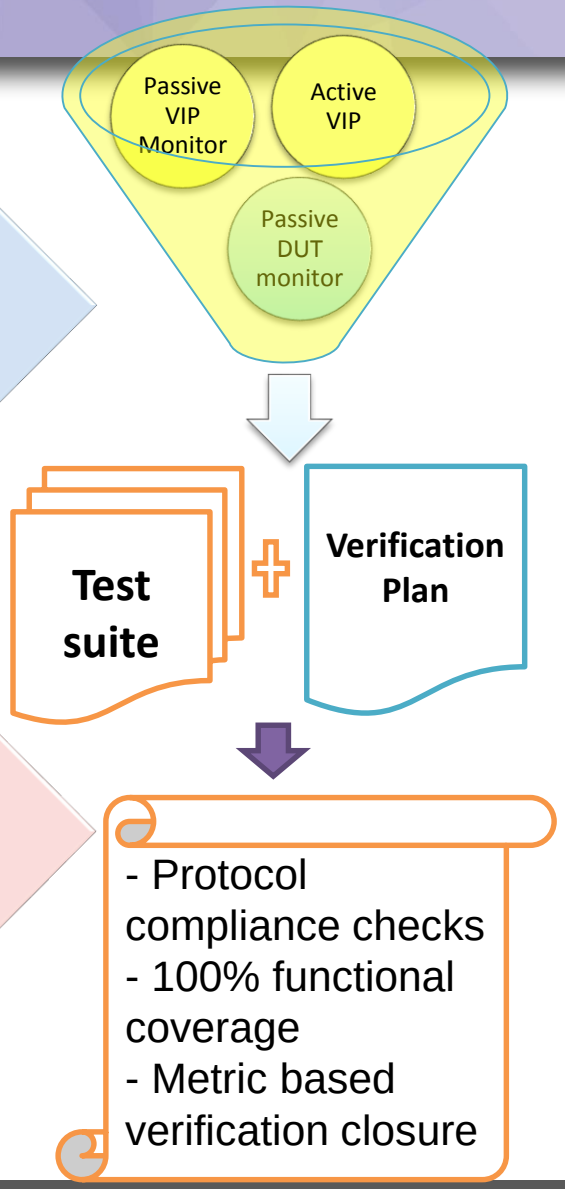
# PCIe Triplecheck

**Setup and configuration**

- Ease of integration
- Automated Verification Plan
- Automated test suite generation

**Test Suite and Vplan**

- Constrained random test suite
- Directed testcases
- Self checking test suite
- Parameterized VPlan



# References

- **PCI Express® Base Specification Revision 4.0 Version 0.7**

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